Notice of Allowability	Application No.	Applicant(s)	
	10/600,491	SACCA ET AL.	
	Examiner	Art Unit	
	Daniel Swerdlow	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 3 November 2005*.

2. ☒ The allowed claim(s) is/are *18,20,22,24,25,28,30 and 32-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Regarding Claim 18, US Patent 5,734,703 to Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: a voltage controlled current source including an operational amplifier (Fig. 9, reference 540) having a positive input connected to a modem output driver (i.e., a transmit signal driver of the modem) (Fig. 9, reference 520; column 18, lines 3-4) with a feedback path from the transistor emitter to the inverting input of the amplifier (i.e., configured to linearly vary a line current of the telephone line); the operational amplifier having an output driving the base of a transistor to form a semiconductor inductor circuit (i.e., an electronic inductor transistor) (Fig. 9, reference 540; column 18, lines 3-4); the transistor connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line). Hiyoshi further discloses the negative input of the operational amplifier connected, via a resistor, to the transistor emitter (Fig. 9, reference 540). US patent 4,796,295 to Gay et al. discloses a telephone interface circuit (Fig. 1) with a transistor (Fig. 1, reference 6) connected to the output of an operational amplifier (Fig. 1, reference 14) driven by an amplifier (Fig. 1, reference 18) that receives a transmit signal (Fig. 1, reference 20; column 3, lines 35-39). As such, the transistor (Fig. 1, reference 6) corresponds to the transistor in Hiyoshi, Fig. 9, reference 540 and to the electronic inductor transistor claimed. Gay further discloses another transistor (Fig. 1, reference 5) with a base connected to the collector of the first (i.e., electronic inductor) transistor. Gay discloses that by driving the second transistor in this way, line current is not drawn until the first (i.e., electronic inductor) transistor is active (column 4, lines 9-16). This avoids leakage currents

that could result in the telephone line spuriously going into an off-hook state, especially when plural devices share a line. Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55). However, Hiyoshi discloses the balancing bridge disposes on the terminal side of the inductor transistor while Gay discloses the balancing bridge on the line side of the corresponding transistor. As such, there is no teaching or suggestion in the prior art or in the knowledge of one of ordinary skill in the art to connect an impedance matching circuit between the positive input of the operational amplifier and the collector of the second transistor, as claimed. Therefore, Claim 18 is allowable.

2. Claims 20, 22 and 24 are allowable due to dependence from Claim 18.

3. Claim 25 contains limitations similar to those of Claim 18 and is allowable for the same reasons.

4. Claims 28, 30 and 32 are allowable due to dependence from Claim 25.

5. Regarding Claim 33, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: modem output driver (i.e., DC loop current) circuit (Fig. 9, reference 520: column 18, lines 3-4) having an operational amplifier (i.e., a first operational amplifier) with a feedback path from the transistor emitter to the inverting input of the amplifier (i.e., configured to linearly vary a line current of the telephone line) having an output connected to the base of a transistor (i.e., a first electronic inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line) and a semiconductor inductor circuit (Fig. 9, reference 540; column 18, lines 3-4) (i.e., AC current circuit) having another operational amplifier (i.e., a second operational amplifier) having an output connected to the base

of a transistor (i.e., a second electronic inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line). However, Hiyoshi discloses the collector of the transistor corresponding to the second electronic inductor transistor connected to the emitter of the transistor corresponding to the first electronic inductor transistor instead of the collector, as claimed. As such, there is no teaching or suggestion in the prior art or in the knowledge of one of ordinary skill in the art to connect the collector of the transistor corresponding to the second electronic inductor transistor to the collector of the transistor corresponding to the first electronic inductor transistor, as claimed. Therefore, Claim 33 is allowable.

6. Claims 34 through 37 are allowable due to dependence from Claim 33.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 571-272-7531. The examiner can normally be reached on Monday through Friday between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Swerdlow
Examiner
Art Unit 2646

ds
27 December 2005